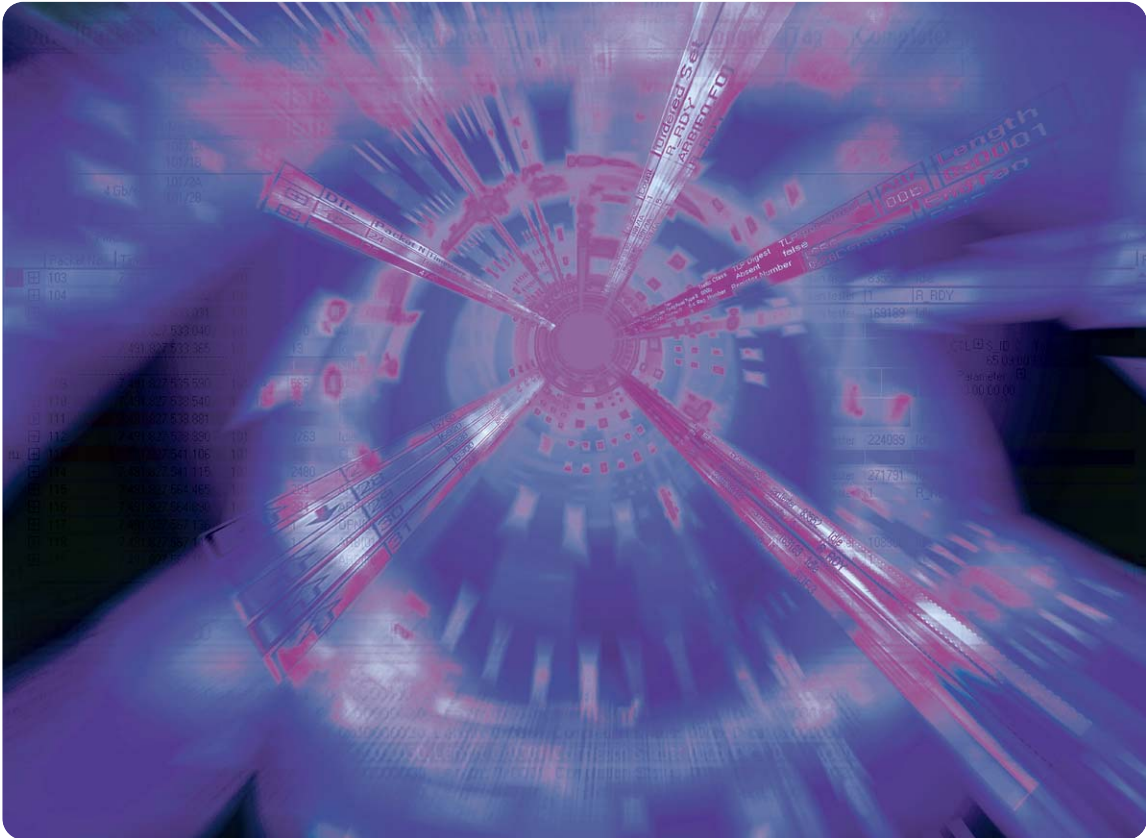
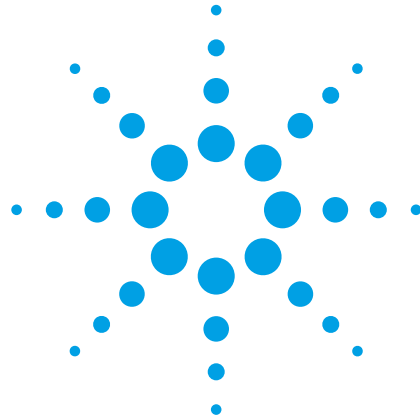


PCI Express® Tools



From the Physical Layer to a Fully Operating System



Agilent Technologies

We're There for Your Evolving PCI Express® Needs

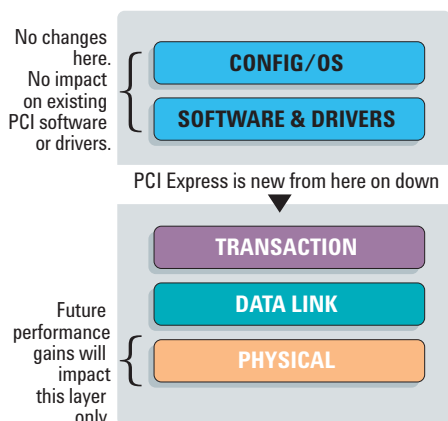


Figure 1. PCI Express layered architecture enables modularity, scalability and re-use.

The increase in required system performance is certainly not over. The expected 1000-fold improvement in the Internet's performance alone will require systems with capabilities beyond what existing buses (ex. PCI or PCI-X®) can provide. When CPU speeds exceed 10 GHz, gigabit networking becomes commonplace, and consumers finally demand high-performance graphics and video, existing bus options will be inadequate.

Many high-speed interconnect technologies are being proposed for use in computer server and desktop systems, but PCI Express is perhaps the most attractive. With an application interface that is consistent with previous PCI implementations, PCI Express allows you to move existing applications and drivers to the next generation of performance without rewriting code.

However, it is not possible to achieve the required performance using existing parallel-bus approaches

without overcoming a signal integrity nightmare. Therefore, an entirely new physical layer is required. PCI Express is based on a 2.5-Gbps serial channel in contrast to the 33/133-MHz multidrop parallel PCI/PCI-X buses. PCI Express can employ up to 32 lanes to push performance up to 80 Gbps. Therefore, you must learn new physical, data link, and transaction layers to implement a system based on PCI Express.

The serial approach makes signal integrity challenges manageable while providing a scalable level of performance by allowing multiple lane deployment. But the serial PCI Express point-to-point architecture also creates complications. A switch must be used to implement multiple boards to emulate a parallel bus.

Agilent Technologies has been deeply involved in the PCI bus since it was first proposed. As a member of the PCI-SIG®, Agilent is continuing its involvement in the development of PCI Express and provides the solutions you need as PCI Express moves into reality.

Physical Layer

With PCI Express, interoperability starts at the physical layer. Development of a PCI Express-based system includes modeling and simulations, but you eventually need to create hardware. You need to validate the integrity of the physical layer and ensure that reflections, crosstalk, emissions, and other effects are within allowable limits. Time-domain reflectometry (TDR) oscilloscopes and multiport vector network analyzers (VNAs) are ideal

tools for evaluating the signal integrity of transmission lines formed within printed circuit boards, and with cables and connectors. Each signal path must be measured to identify impedance discontinuities and losses that might render a signal path useless. Beyond testing signal paths, you must also check lane-to-lane skew, analyze jitter, and measure drive strength and receiver tolerance. The logical sub-block of the physical layer includes link initialization and training that must be validated prior to moving data.

The Agilent Infiniium DSO80000 Series 13 GHz real-time oscilloscope offers up to 40 GSa/s with 2M of memory. The 12 GHz 1169A InfiniiMax active differential and single-ended probes offer unsurpassed performance, accuracy and connectivity for real-time signal integrity measurement of the PCI Express physical layer. The flexible architecture of the InfiniiMax active probes allow you to make measurements with a hand held browser, solder in, socketed or SMA connection for both differential, as well as single-ended measurements.

The Agilent 86100B digital communications analyzer has the bandwidth and TDR functions you need to perform these measurements. The Agilent physical-layer test systems, based on a VNA, are very powerful tools for characterizing signal paths and creating time-domain waveforms of high accuracy and resolution. The Agilent 81133/34A 3.35-GHz pulse/pattern generator is ideal for PCI Express driver and receiver validation.

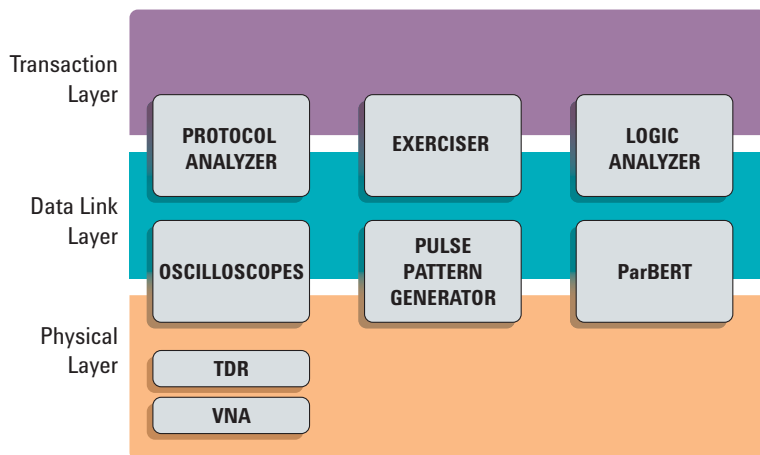


Figure 2. Agilent offers test tools for PCI Express physical, data link, and transaction layers.

Data Link Layer

The data link layer ensures that data is reliably delivered to its destination via the PCI Express link. The major goal of the data link layer is data integrity. Once the physical layer is validated, the data link layer must be validated. Because PCI Express adds a sequence number and CRC to the transaction-layer packet, validating the data link layer is not trivial. It is necessary to use capable test tools that will allow you to monitor data movement and provide consistent stress to fully test the data link.

PCI Express includes a flow-control protocol to ensure that packets are only transmitted when there is buffer space to receive them. This is intended to reduce the number of packet resends due to buffer overruns. It is important to measure the implementation of the optimized buffer depth (and performance), virtual lane correctness, CRC operation, link training, and proper flow control. An Agilent 16900 Series logic analysis system with a

packet analysis probe will ease the process by allowing you to trace link traffic at the protocol level with a fully decoded packet display and packet triggering.

PCI Express exerciser and protocol analyzer solutions from Agilent assist your development of silicon, add-in cards, servers, and workstations. Their modular and flexible architectures allow for continuous feature upgrades. These tools can be used for functional validation, exercising protocol variations, error insertion, automated compliance tests, device emulation, stress testing, generating and receiving maximum-bandwidth traffic, protocol observation, and emulating multiple streams and virtual lanes. They provide comprehensive test coverage with repeatable and deterministic test scenarios.

Transaction Layer

The transaction layer receives read and write requests from the

application software in the same way as PCI and PCI-X. All of these requests are implemented as split transactions, and some of the request packets require a corresponding response packet. Also, the transaction layer receives response packets and has to match these with the appropriate request packets (each packet has a unique identifier that enables response packets to be directed to the correct originator). Packets have attributes that may be used to optimally route these packets through the I/O subsystem.

Such a complex transaction layer can be debugged and validated with the Agilent 16900 Series logic analysis system with a packet analysis probe. The E2960 Series provides the industry's first full-speed x1, x2, x4 and x8 combined exerciser-analyzer platform, which provides R&D and QA engineers with bring-up, debug and validation capabilities to test and validate hardware and software designs.

The traffic flowing over PCI Express links almost always comes from and goes to other buses, such as the CPU front side bus, memory, InfiniBand, PCI and PCI-X, Serial ATA, AGP 3.0, and other I/O buses. The ability to simultaneously trace activity on these buses as well as PCI Express is crucial when validating the complete system. The Agilent 16900 Series logic analysis systems provide support for virtually every bus in the system, making it easy to follow transactions, data and packets as they flow through the system. The system performance analysis (SPA) tool set identifies elusive bottlenecks so you can optimize system parameters and architecture.

Physical Layer Design, Validation and Modeling



Physical Layer

High-speed system design starts with the physical structure. PCI Express data rates are equivalent to sending microwave signals through copper structures. First-pass success demands a systematic approach to design and validation. Microwave engineers have addressed similar design challenges by breaking down the system to model each component separately, then together as a complete channel.

Accurate simulations require accurate component models. You can modify existing models or rely on supplied libraries but the most accurate method is to measure actual components. Measurement-based models increase your confidence by providing real-world data to your time domain or frequency domain simulator.

Each channel must handle data rates in excess of 2.5 Gbit/sec to ensure sufficient margins to cover for manufacturing and process variations, connector wear and silicon aging. A good rule of thumb is 10-25% margins.

Characterize your design and extract models with either a TDR (time domain reflectometer) or a 4-port VNA (vector network analyzer). Both offer advantages and produce similar results. TDRs are more affordable and often familiar while VNAs are capable of more accurate and traceable results.

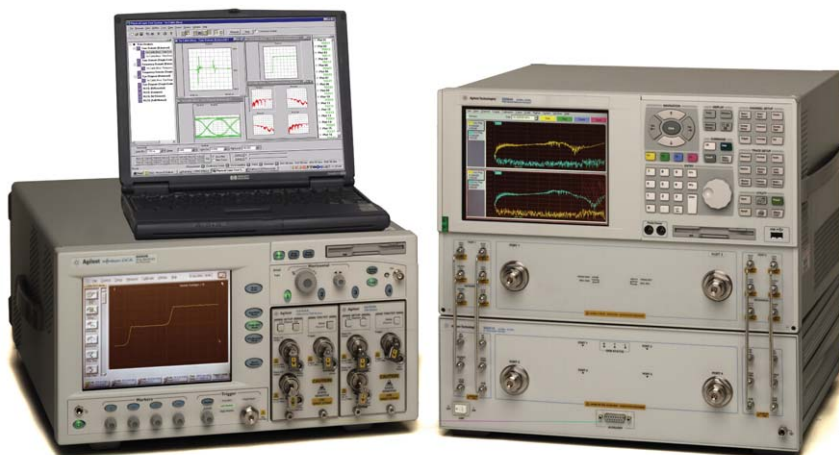


Figure 3. Both the TDR and VNA provide accurate results of the PCI Express physical layer.

Application	Typical Measurements	Recommended Solution(s)
PCI Express Component Development	Build, validate and de-embed test fixture Complete characterization Data export to model extraction & analysis products	PLTS w/VNA
Incoming Inspection of PCI Express Components	Validate vendor-supplied component samples Model extraction for system simulation	PLTS w/TDR PLTS w/PNA or ENA alone
System Validation	Complete validation of your PCI Express channel; including SDD21 and SDD11 measurements	PLTS w/TDR or VNA
One Time Measurement Need	Extract channel or device models Validate PCI Express conformance	Model Extraction Services from Agilent Technologies (see pages 12 and 13)

Table 1. PCI Express Physical Layer Test Solutions.

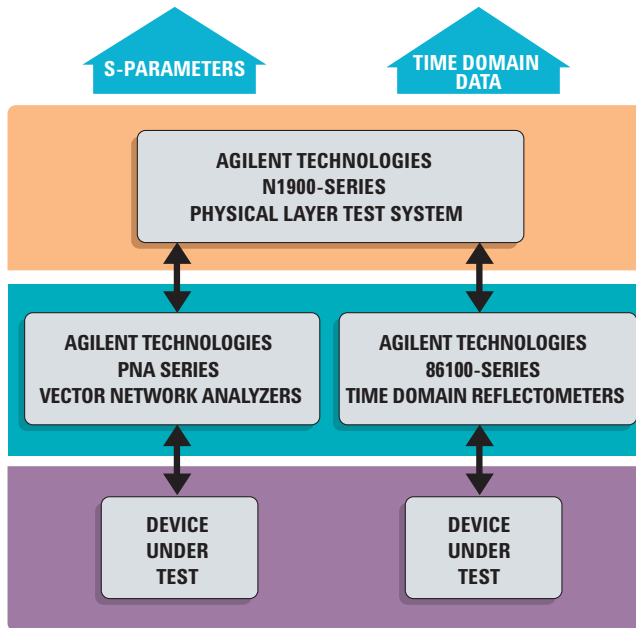


Figure 4. The Agilent PLTS enables you to control, measure and compare data from both TDR and VNAs.

The Agilent TDR/TDT

A TDR combines a sampling oscilloscope with a step generator capable of launching a fast edge into the device under test (DUT). The reflected wave (TDR) displays impedance discontinuities through the structure of the device. The transmitted wave (TDT) enables you to measure system loss and propagation delay.

To obtain greater accuracy, use TDR/TDT Normalization. Normalization goes beyond traditional vertical and time base calibrations to remove electrical delay and loss of your cable from measurement results.

The Agilent 86100B Infiniium digital communications analyzer (DCA), and 54754A differential time domain reflectometer module are intuitive

tools for debug, analysis and model extraction. Oscilloscope measurements and eye diagrams are available when the TDR is turned off. Excess inductance and capacitance measurements determine the location and magnitude of discontinuities.

The Agilent 4-Port Vector Network Analyzer (VNA)

A VNA uses stimulus/response to characterize the DUT. A sine wave is transmitted into the DUT while tuned receivers are swept in lockstep, providing both reflection and transmission properties. VNAs offer greater measurement resolution and accuracy than a TDR through calibration and fixture removal techniques that have been refined through years of demanding microwave applications. VNA results

are calibrated using frequency domain artifacts – each measurement is accurate, repeatable and traceable to industry standards.

VNA measurements are usually expressed as Scattering Parameters (or S-Parameters) which can be translated into time-domain views. S-Parameters are well established as the best technique to characterize the manner in which a PCI component modifies a digital signal.

The Agilent Physical Layer Test System

The physical layer test system (PLTS) provides confidence through complete characterization and model extraction of your DUT. PLTS supports both the TDR and VNA measurement platforms, providing instrument control including setup, error correction, acquisition, analysis and data transfer – thus reducing the difficult and time-consuming process of measuring differential structures to a few keystrokes and reducing the chance of error.

PCI Express requires characterization of input differential insertion and loss and near/far end crosstalk. PLTS provides direct measurement of insertion and return loss, as well as mode conversion analysis, which is used to determine cross-talk.

Guided setup and calibration methodologies ensure that the data you capture accurately reflects your DUT. Export VNA or TDR data to simulators that accept S-Parameters or to TDA Systems IConnect model extraction and analysis software.

Oscilloscopes and Probes



The Agilent Infiniium DSO80000 Series oscilloscope system provides unmatched accuracy, performance and connectivity for signal integrity measurements on PCI Express signals. It offers up to 13-GHz bandwidth with two channels, each sampling at 40 GSa/s with 2 M of memory. The award-winning InfiniiMax 13 GHz active differential and single-ended probe system offers connection flexibility, with hand held browsers, solder in, socketed and SMA connections. PCI Express signals have approximate rise and fall times of 125 ps, which requires a minimum 6 GHz bandwidth and 20 GSa/s sampling rate essential for accurate measurements of rise times and eye opening.

The jitter budget for TJ for PCI Express signals is small – on the order of 87 ps (BER 10^{-6}) maximum under the 1.1 specification. An oscilloscope with low trigger jitter and jitter noise floor is essential to characterize the true jitter margin. The trigger jitter of the DSO80000 Series is < 0.5 ps rms and the jitter measurement noise floor for time interval error measurements is as low as < 0.65 ps rms.

With PCI Express, you often only want to use as much bandwidth as necessary and with the Agilent DSO80000 Series you have the optional capability to utilize the full 40 GSa/s sample rate in a proprietary noise reduction mode that allows the scope to have a lower overall bandwidth coupled with an even lower DSP reduced noise floor. This can provide you with a much more accurate measurement in systems where vertical noise is an issue.

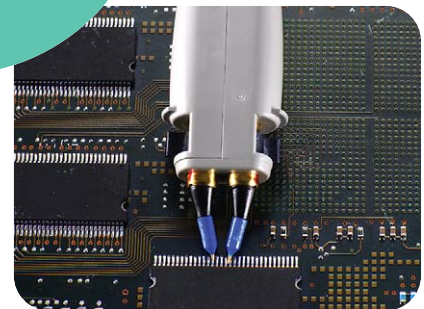
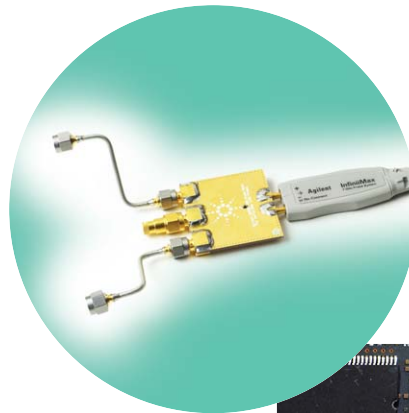


Figure 5. The Agilent DSO80000 Series oscilloscopes and InfiniiMax Series probes deliver a high-performance, 13 GHz, end-to-end measurement system.

Probing PCI Express signals on a printed circuit board or IC package is extremely challenging, because the PCI Express signals are high speed and are differential. The Agilent 1169A 13-GHz InfiniiMax differential probe system ensures accurate differential measurements with a 12 GHz system bandwidth and flat response at the probe tip. The DS0801304A scope and 1169A active differential probe can be used to measure the following parameters specified in the *PCI Express Physical Layer Specification*:

- Unit interval
- Differential peak-to-peak output voltage
- Minimum TX (transmitted) eye width
- Maximum time between the jitter median and maximum deviation from the median
- D+/D- (differential plus/differential minus) TX output rise/fall time
- ac peak common mode output voltage
- Absolute delta between dc common mode during LO and electrical idle
- Absolute delta between dc common mode between D+ and D-
- Electrical idle differential peak output voltage
- Amount of common mode voltage change allowed during receiver detection
- Minimum time spent in electrical idle.

The Agilent Technologies N5393A PCI Express electrical performance validation and compliance software provides you with a fast and easy way to verify and debug your PCI Express designs. The N5393A PCI Express electrical test software utilizes the clock recovery method used in the official PCI-SIG Signal Quality Test Methodology (“SigTest”) application, ensuring that your test results are consistent with results from the SigTest application. The N5393A requires the E2688A serial data analysis software and one of the PCI-SIG approved compliance test fixtures (CBB or CLB).

Features:

- Test setup wizard guides you through test selection, configuration, connection, execution, and results reporting.
- PCI-SIG SigTest clock recovery algorithm is used to ensure consistency with SigTest.
- Measurement connection setups are displayed when you must change the test setup.
- Oscilloscope setup is automatically configured for each test.
- Test results report formally documents your test configuration, measurements made, pass/fail status, and waveforms.
- Pass/fail margin analysis provides an indication of how close your device is to meeting a test specification.

The Agilent E2688A serial data analysis package for the Infiniium real-time oscilloscope offers clock recovery and mask templates for PCI Express, as well as other popular serial buses, such as Serial ATA, Fibre Channel and Gigabit Ethernet. The E2688A allows you to easily perform pass/fail mask testing on the PCI Express physical layer.

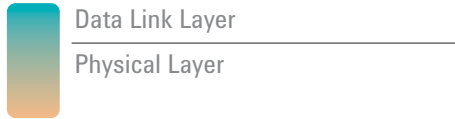
PCI Express 1.1 Testing

Testing of PCI Express under the 1.1 revision requires the use of a clean clock source. For testing add-in cards a 1.1 compatible CBB with a clean clock oscillator is available from the PCI-SIG. In addition, jitter measurements using this version of the CBB are made using a clock recovery function specified as a first order PLL response with a corner frequency at 1.5 MHz.

PLL Loop bandwidth tests for add-in cards can also be made with this board using an Agilent E4440A spectrum analyzer and an E8267D PSG vector signal generator.

For lower speed reference clock testing, the DS080000 Series supports a very long memory capture of up to 64 M points. Agilent recommends using 4 GSa/s sample rate to capture 2 GHz of bandwidth for this signal. This gives you excellent spectral data to perform the necessary band pass filtering required for the phase jitter measurement.

Pulse/Pattern Generator



Validating the receiver side of PCI Express designs is often more challenging than testing the transmitter side. With an Agilent 81134A pulse/pattern generator, signals and data sequences or test sequences can be generated that stimulate the PCI Express device under test (DUT). This DUT, in turn, responds by outputting a similar sequence—the bit flow of the answer is predictable and can be measured by a logic analyzer. This behavior can be used to characterize the receiver input performance.

The training sequence can be sent as a clean signal or with stress applied to it. For functional testing, the 81134A pulse/pattern generator provides clean signals with low noise and low jitter, exceeding the minimum requirements defined in the PCI Express standard. Stress measurements are made by reducing the levels/swing below the minimum requirements of the receiver. The Agilent 81134A, in combination with a function generator, generate the stress. For testing PCI Express x4, x8, and x16, the scalable 81250 ParBERT platform is the ideal solution for making functional and stress tests on multiple channels (up to 64 channels).



Figure 6. Generate training sequences with or without stress for driver and receiver validation.

Description	Measure	Equipment	Compliance
Receiver voltage	Application of training sequence, detection of answer	Pulse/pattern generator, logic analyzer	RX eye
Jitter outlier (Tolerance)	Eye modulation	Same as above plus function generator	Jitter budget, section 4.3.4
Common mode	Common mode noise	Same as above	Common mode noise < 100 mV, section 4.3.4
Crosstalk on idle	Single-ended noise	Same as above	Noise < 65 mV, section 4.3.3
Delay between lanes	Multiple lane stimulus	ParBERT 81250	< 20 ns any lane per port

Table 2. The Agilent 81134A pulse/pattern generator enables design validation and compliance measurements at the receiver.

Parallel Bit Error Ratio Tester



Increasing speed rate for PCI Express II is driving designs to new dimensions. Validating and testing of PCI Express devices at the physical layer is getting more and more challenging for today's engineers.

The important test requirement is measuring BER on the PCI Express I/O ports. The PCI Express design works in loopback mode for characterization. The Agilent ParBERT 81250 platform provides standard compliant training sequences, compliance patterns and SKP frames to stimulate PCI Express design. The bit flow can be controlled and combined by the ParBERT sequence editor to a complex data flow including loop level control.

For testing and validating the PCI Express receiver site, the ParBERT 81250 is able to provide a very clean data signal with low noise and jitter. Conversely, ParBERT is flexible in creating a differential de-emphasized data signal including large eye closure by jitter modulation. For data analysis, ParBERT provides differential connectivity and CDR. The ParBERT 81250, in combination with a function generator, can modulate a defined jitter amplitude to test minimum receiver eye width characteristics and jitter tolerance measurements. Spread spectrum clocking is achieved by frequency modulation of clock and data. For testing PCI Express x4, x8 and x16, multiple stimulus channels can be configured for functional and stress test on multiple channels.

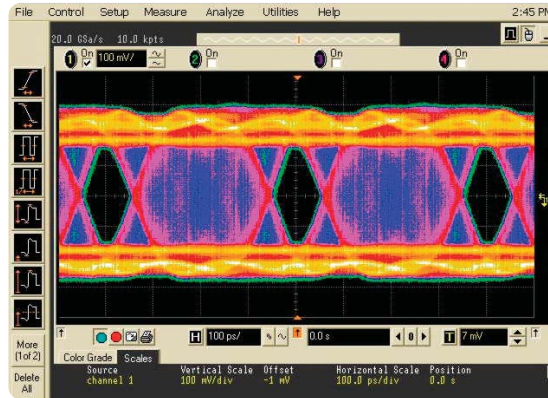


Figure 7. De-emphasized signal with jitter modulation.

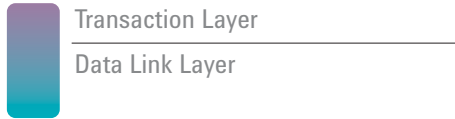
Required feature set	Compliance / test need
Differential de-emphasis TS1, TS2, SKP, compliance patterns	RX data detection
Jitter modulation	Minimum detectable eye width jitter tolerance
Frequency modulation @ clock/data	Spread spectrum clocking (SSC)
Multiple lane stimulus	Measure delay between Lanes x4,x8,x16
Sequence editor to generate PCI Express training sequences	Set device into loopback mode
Differential analysis with CDR	BER measurement
Speed rate up to 7 Gbit/s	Support for PCI II

Table 3.



Figure 8. Multi channel ParBERT system generates training sequences and controls PCI express into loopback mode for standard compliance measurements.

Protocol Analyzer and Protocol Exerciser



The new Agilent Technologies system protocol tester is comprised of a protocol analyzer and protocol exerciser for PCI Express. The tools enable users to exercise and analyze bus protocols on the data link and transaction layers and provide bring-up, debug, validation and compliance testing capabilities. They are ideal tools for R&D and QA engineers who are developing hardware and software designs for PCI Express systems spanning the entire computer industry, including semiconductors, chips, motherboards, BIOS, drivers, servers and add-in cards.

“Support for PCI Express x8 technology will accelerate development of enterprise systems and adapters enabled by the serial I/O technology,” said Jim Pappas, director of initiative marketing, Intel Enterprise Platform Group. “The demonstrations at the PCI-SIG Developers Conference and Agilent’s aggressive delivery of PCI Express testing suites are important steps for the industry.”

The Agilent E2960-E08 protocol exerciser is used to test and validate x1, x2, x4 or x8 PCI Express designs. It can interactively generate and respond to arbitrary transactions as well as test corner cases and behavior by inserting error conditions and protocol violations and monitor the system in response to these errors.

- Command Application Programming Interface (CAPI) for automated testing (C++ and TCL programming interfaces)
- Error insertion

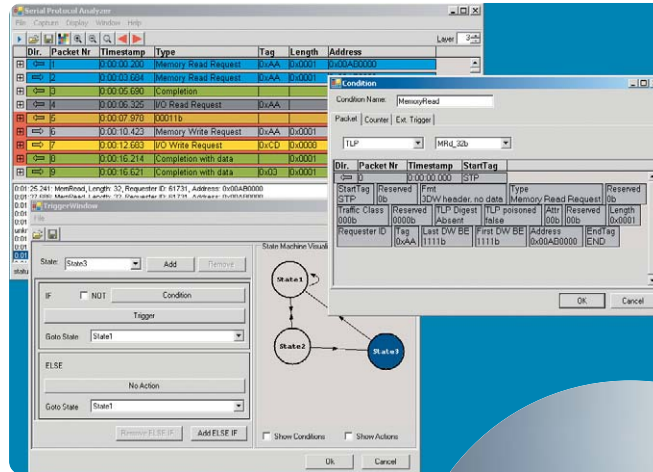


Figure 9. The system protocol tester provides increased test coverage for higher test quality, reducing the risk of costly recalls and redesigns and faster test times, enabling faster time-to-market.



- Can act as an end-node (for platform testing) or act as a root-complex (for add-in card testing)
- Emulation of configuration space of a switch
- Compliance test capabilities
- LAN interface for remote control

The Agilent E2960-A08 protocol analyzer provides non-intrusive monitoring of captured PCI Express traffic between an adapter card and a system or between an external PCI Express device and a system. It is involved in bring-up and debug of PCI Express designs and includes an intuitive graphical user interface with search and display filter capabilities.

- Link training analysis, root cause analysis and troubleshoot problems
- Patented “Dynamic Trigger

Conditions” for simplified triggering on sophisticated transactions (Dynamic pattern terms is a patented technology that allows the user to trigger on a certain part of a packet where the content is determined at runtime)

- Protocol exerciser as controlled end node stimulus to complement protocol analyzer – all in one frame
- Hierarchical views (byte / packet / transaction)
- LAN interface for remote control and to share applications
- Captures data link layer packets and transaction layer packets
- Bi-directional, interleaved display, including time-stamps
- Dedicated PCI Express trigger and storage qualification

Protocol Compliance Test Card



Transaction Layer

Data Link Layer

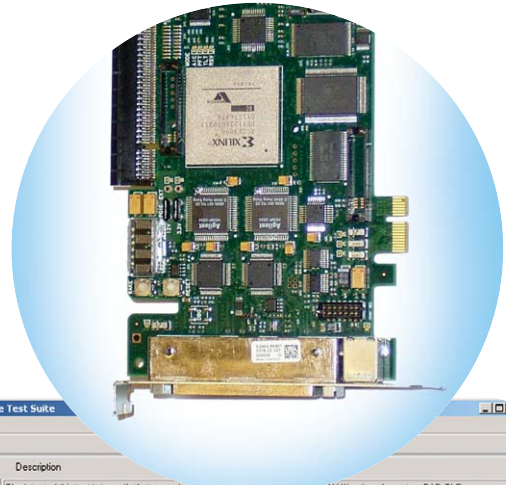
The Agilent E2969A protocol test card performs tests to verify and ensure compliance with PCI Express as defined by the PCI-SIG. In addition, the card also guarantees the interoperability of the DUT with other PCI Express devices. It is primarily for use by R&D engineers who wish to validate the functional compliance of their PCI Express-based designs, including chips, add-in cards or systems.

The E2969A protocol test card is a collaborative development between Agilent and Intel that coincides with the Intel product development solution for the PCI Express market.

- Automated pre-programmed compliance tests for the transaction and data link layer
- Tests power management and configuration space
- Carefully monitors the behavior of the DUT in response to certain error conditions
- Connection to protocol analyzer
- Known endpoint and switch functionality
- Field upgradeable FPGA-based card
- USB 2.0 interface for programming and topology simulation mode
- Supports add-in cards with up to x16 lane width
- Can act either as a PCI Express standalone add-in card, or as a PCI Express interposer card for x1 operation
- Card controlled via PCI Express or via an external host

The protocol test card provides three test modes. During the add-in card test mode, the card is plugged in between the system and the add-in card. It monitors the behavior of the add-in card, its device drivers and operating system in response to a range of inserted errors. The platform test mode monitors the behavior of the platform, its device drivers and OS, also in response to various

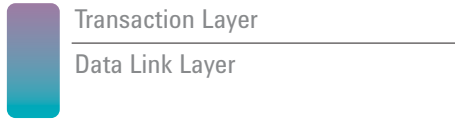
error conditions. During the topology simulation mode, the protocol test card appears as a complex PCI Express topology. It aids in verifying the PCI Express compliance of the BIOS, so that it is able to detect and initialize a complex PCI Express topology.



Execute	Status	Category	Name	Description
<input type="checkbox"/>	PASSED	Link	BadCRC_EP_USW	The intent of this test is to verify that a receiver...
<input type="checkbox"/>	FAILED	Transaction	CompletionTimeout_TxN_BFT_EP	Verify Basic Completion Timer requirements of a slotted Endpoint device. The Completion Timeout timer must not expire in less th...
<input type="checkbox"/>	PASSED	Link	ComputedDLLPs_EP_USW	The intent of this test is to ensure that a DUT recognizes a DLLP with bad CRC, drops it and logs a BAD_DLLP port error.
<input type="checkbox"/>	PASSED	Link	DuplicateTLPSeqNum_EP_USW	The intent of this test is to verify that the duplicate TLP with the same sequence number associated at the link layer as that in th...
<input type="checkbox"/>	PASSED	Link	LinkRetrainOnRetryFailNoAckNack_E	The intent of this test is to ensure that the link connected to the DUT will go into retraining after trying for REPLAY_NUM of time...
<input type="checkbox"/>	PASSED	Link	LinkRetrainOnRetryFail_EP_USW	The intent of this test is to ensure that the link connected to the DUT will go into retraining after trying for REPLAY_NUM of time...
<input type="checkbox"/>	FAILED	Transaction	NegotiatedLinkWidth_TxN_BFT_EP	The intent of this test is to ensure that the link connected to the DUT will go into retraining after trying for REPLAY_NUM of time...
<input type="checkbox"/>	PASSED	Link	RetrainOnNak_EP_USW	The intent of this test is to ensure that the link connected to the DUT will go into retraining after trying for REPLAY_NUM of time...
<input type="checkbox"/>	PASSED	Link	ReplayNumTest_EP_USW	ReplayNumTest (Test5220) If repeated retries fail and REPLAY_NUM overflows, the link transmitter must ask the Physical Layer to retrain the link. There must be a reported error to correspond to this as per Section 5.2 (DLL 5.287 (Test5220))
<input type="checkbox"/>	n/a	Transaction	RequestCompletion_TxN_BFT_EP	The link state (including the contents of retry buffer) must not change in link retraining if Physical LinkUp=1.
<input type="checkbox"/>	PASSED	Link	ReservedFieldsDLLPReceive_EP_US	The intent of this test is to verify that the DUT truly ignores reserved fields in an ACK DLLP by sending arbitrary data in those fiel...
<input type="checkbox"/>	n/a	Link	UndefinedDLLPEncoding_EP_USW	The intent of this test is to verify that the DUT silently drops any DLLP with undefined encoding (any pattern for DLLP type that i...
<input type="checkbox"/>	n/a	Link	WrongSeqNumInAckDLLP_EP_USW	The intent of this test is to verify that the DUT drops any ACK DLLP that doesn't have a sequence number corresponding to an...

Figure 10. Easily validate the functional compliance of your PCI Express-based designs with the E2969A protocol test card.

Logic Analysis System



Proper system validation underscores the need for full system visibility. The traffic flowing over PCI Express links usually travels to and from other buses, such as the CPU front side bus, memory, InfiniBand, PCI and PCI-X, Serial ATA, and AGP 3.0. The ability to simultaneously trace activity on these buses, as well as PCI Express, is crucial when validating the complete system.

The N4220B packet analysis probe captures PCI Express traffic and, coupled with a 16900 Series mainframe and the 1695X or 16753/54/55/56A logic analyzer modules, provides triggering, cross-correlation, and detailed measurements for complete PCI Express system hardware and software debugging.

The PCI Express architecture is scalable and extensible, and includes a rich set of features. It supports multiple interconnect options, such as the slot connection and chip-to-chip interconnect. PCI Express has a variety of link widths from x1 through x16. These bus features, in addition to the heavy protocol nature of PCI Express, require the ability to set up your traces, your triggers and your packet view of the traffic on the link at the protocol level.

PCI Express has many interesting features that require validation at the various layers. Common areas for investigation include squelch mode, power-down mode, decode of the 10b codes to 8b traffic, various link training sequences, different kinds of packets, spread spectrum clocking, and data scrambling



Figure 11. Optimize your PCI Express validation efforts with a low-intrusion, easy-to-use packet analysis probe.

Figure 12. Achieve low loading (<0.7 pF), an easy connection and a small footprint with soft touch connectorless probes.

employed to reduce EMI emissions from PCI Express implementations.

Traditionally a logic analyzer has been used to look into multiple points in a complete system so it can perform all of the measurements that you need for full validation. Due to the serial nature of PCI Express, the logic analyzer must now handle not only the traditional parallel common clock and source synchronous clock buses, but also these very high-speed, multi-lane, packet-oriented, embedded clock serial buses.

The first major challenge encountered while probing PCI Express is the physical access to the signals. When you are doing point-to-point connections between chips, it

becomes necessary to physically probe the traces that go between the chips. Agilent's new soft touch connectorless probing technology helps overcome this challenge. With extremely low loading, soft touch provides a space-saving, pre-defined printed circuit board footprint you can design into your board. The Agilent soft touch probe for PCI Express uses light compression technology on the exposed area of your circuit board and picks up the signals as they travel from chip to chip. When a footprint isn't available, the Agilent N4221F flying lead probe set allows you to probe a chip-to-chip link up to x16 without a midbus footprint. For developers of PCI Express slot connectors, a low intrusion interposer is also available.

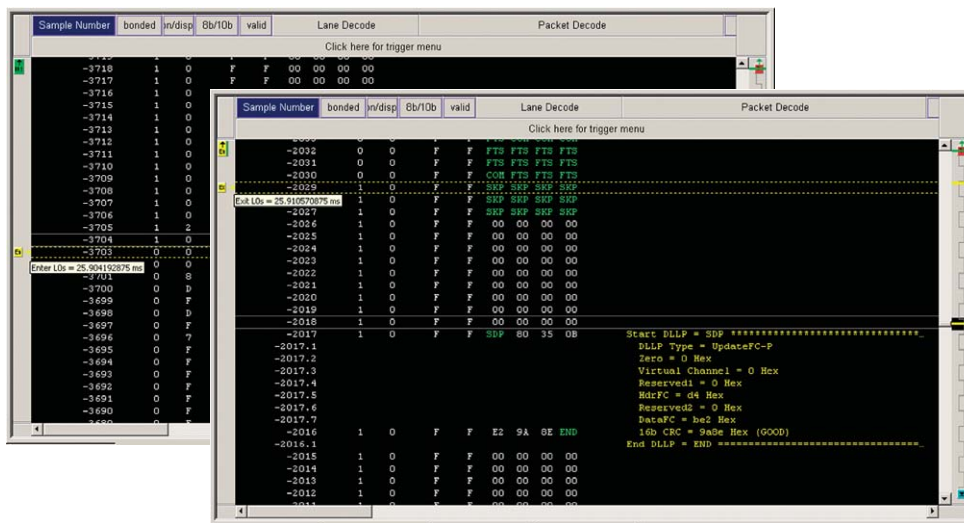


Figure 13. With L0s power management mode, bit lock is acquired in 48 symbols (192 ns) the fastest in the industry, and critical for L0s' capture.

The nature of PCI Express protocol also adds to the validation complexity. The PCI Express traffic on the bus consists of encoded packets that are placed into serial bit streams with data scrambling and spread spectrum clocks. It's essential that the logic analyzer removes all of that complexity from the trigger setup.

The Agilent N4220B Series packet analysis probes provide you an intuitive GUI (graphical user

interface) so you can quickly and easily define the different kinds of PCI Express packets. You can select the kind of packet you want the logic analyzer to look for to help you examine the link operation in real time and identify that packet when it crosses the link.

The final step in validating your PCI Express system is to actually view the trace results. The Agilent N4220B Series of analysis

probes includes a Packet Viewer software that handles format details, including lane deskew, data scrambling and data format. The ability to view raw 8b and/or 10b codes is still retained. This complements the packet analysis capability Agilent provides for other buses, such as serial ATA and InfiniBand, but is even more powerful due to the wide-lane feature of PCI Express.



Figure 14. Troubleshoot the transaction and data links of PCI Express buses more economically with the 16800 logic analyzer and the Agilent FSI-60112 packet analysis probe.

A lower-cost approach for PCI Express validation

The Agilent FSI-60112 packet analysis probe with the 16800 Series portable logic analyzer is another alternative to achieve similar PCI Express traffic captures for up to x4 link widths at a lower cost. The midbus probe, slot interposer and flying lead set probes provides connections with chip-to-chip,

chip-to-slot and slot-to-slot PCI Express architecture. The solution also includes protocol decode with the Packet Viewer and Transaction Viewer software. Transaction Viewer is a new way of displaying bus transactions at high-level summary view to quickly scan transactions and expose lower details of transactions of interest with the drill-down feature.

Test and Measurement Engineering Services



Figure 15. You will benefit from a wide variety of tools and broad expertise when you use Agilent's measurement services.

Agilent offers a comprehensive set of services to help accelerate your time to market and ensure the successful development of your PCI Express design. Gain quick access to Agilent's experts and newest technologies. Tap into a deep well of expertise and tools gleaned from Agilent's 60 years of test and measurement experience. Whether you want to outsource your test, build your in-house test capability, get help with test planning, or just learn more about PCI Express, Agilent is ready to work for you.

Technology Training

Ramp up on PCI Express quickly. If you are responsible for validation, debug or compliance testing, our PCI Express training courses will help you succeed. After completion of the course you will have mastery of the PCI Express specification and you'll be equipped to develop your product test plan.

Test Plan Development

As you push the envelope on product development, design and planning for test is paramount. Agilent's knowledge and expertise can help ensure you're ready.

Agilent's Product Training and Application Services

Agilent's broad range of services will help you get the most out of your PCI Express development tools. Our flexible productivity assistance offerings can be custom-tailored to help your organization with anything from ensuring the proper configuration and installation of your equipment, to assisting you with test and debug of your product. We also offer a number of quality training courses to help you fully understand the measurement capabilities of your tools, accelerating your ramp-up time significantly.

Outsourcing

With Agilent Measurement Outsourcing Services, Agilent becomes an extension of your design validation/test process. Agilent's Measurement services provide flexible access to Agilent expertise and technology. Our services lower the overall cost of your validation and test processes by allowing you to:

- Use operational money instead of capital.
- Have the correct resource, with the right expertise, when and where you need them.
- Have higher utilization of test equipment in the lab.
- Evaluate the feasibility of a test technology before making a larger investment

For more information about Agilent's professional engineering services, log onto www.agilent.com/find/usproducts_services

Stay Ahead of Emerging Technologies

Conclusion

Agilent has been there for you in the past and will continue to be there as PCI Express evolves. Agilent is committed to providing the PCI Express test tools you need. With the experience gained developing PCI/PCI-X and InfiniBand tools, Agilent is well positioned and ready to provide the best solutions for this evolving interconnect technology.



Related Literature

<i>86100B Agilent Infiniium DCA</i>	Color Brochure	5988-5235EN
<i>16800 Series Portable Logic Analyzer</i>	Color Brochure	5989-5062EN
<i>16900 Series Logic Analysis System</i>	Color Brochure	5989-0420EN
<i>N4220B Packet Analysis Probe</i>	Technical Overview	5989-0086EN
<i>FSI-60112 Packet Analysis Probe for PCI Express</i>	Data Sheet	5989-5584EN
<i>81133A and 81134A Pulse/Pattern Generators</i>	Data Sheet	5988-5549EN
<i>Physical Layer Test Systems</i>	Data Sheet	5988-5288EN
<i>Physical Layer Test System (PLTS Version 3.0)</i>	Technical Overview	5989-0271EN
<i>Infiniium 80000 Series Oscilloscopes InfiniMax II Series Probes</i>	Data Sheet	5989-1487EN
<i>PCI Express Receiver Design Validation</i>	Application Note	5988-7432EN
<i>ParBERT 81250 Parallel Bit Error Ratio Tester</i>	Data Sheet	5968-9188E
<i>E2960 Series System Protocol Tester for PCI Express</i>	Color Brochure	5989-2526EN
<i>Jitter Solutions for Digital Circuits</i>	Color Brochure	5988-8427EN
<i>Agilent's High Speed Physical Layer Characterization and Modeling Service</i>	Technical Overview	5988-7042EN



Agilent Email Updates

www.agilent.com/find/emailupdates

Get the latest information on the products and applications you select.



Agilent Direct

www.agilent.com/find/quick

Quickly choose and use your test equipment solutions with confidence.



www.agilent.com/find/open

Agilent Open simplifies the process of connecting and programming test systems to help engineers design, validate and manufacture electronic products. Agilent offers open connectivity for a broad range of system-ready instruments, open industry software, PC-standard I/O and global support, which are combined to more easily integrate test system development.

PCI Express[®], PCI-X[®] and PCI-SIG[®] are registered trademarks of PCI-SIG.

For more information on PCI Express tools visit

www.agilent.com/find/pci_express

Remove all doubt

Our repair and calibration services will get your equipment back to you, performing like new, when promised. You will get full value out of your Agilent equipment throughout its lifetime. Your equipment will be serviced by Agilent-trained technicians using the latest factory calibration procedures, automated repair diagnostics and genuine parts. You will always have the utmost confidence in your measurements.

Agilent offers a wide range of additional expert test and measurement services for your equipment, including initial start-up assistance onsite education and training, as well as design, system integration, and project management.

For more information on repair and calibration services, go to

www.agilent.com/find/removealldoubt

www.agilent.com

For more information on Agilent Technologies' products, applications or services, please contact your local Agilent office. The complete list is available at:

www.agilent.com/find/contactus

Phone or Fax

United States:

(tel) 800 829 4444

(fax) 800 829 4433

Canada:

(tel) 877 894 4414

(fax) 800 746 4866

China:

(tel) 800 810 0189

(fax) 800 820 2816

Europe:

(tel) 31 20 547 2111

Japan:

(tel) (81) 426 56 7832

(fax) (81) 426 56 7840

Korea:

(tel) (080) 769 0800

(fax) (080) 769 0900

Latin America:

(tel) (305) 269 7500

Taiwan:

(tel) 0800 047 866

(fax) 0800 286 331

Other Asia Pacific Countries:

(tel) (65) 6375 8100

(fax) (65) 6755 0042

Email: tm_ap@agilent.com

Revised: 09/14/06

Product specifications and descriptions in this document subject to change without notice.

© Agilent Technologies, Inc. 2005, 2006

Printed in USA, October 2, 2006

5988-7780EN



Agilent Technologies