

D3186 Specifications

Operating Clock

Operating clock source:	Internal clock (optional), external clock
Internal Clock (optional)	
Frequency range:	150 MHz to 12 GHz (Option 10) 150 MHz to 12.5 GHz (Option 13)
Frequency setting resolution:	1 kHz
Frequency stability:	±10 ppm/year
Output waveform:	Sine wave, approx. 1 Vp-p
Spurious:	-37 dBc (non harmonic wave)
SSB phase noise:	-70 dBc/Hz (10 kHz offset, 12 GHz carrier)
Frequency memory:	16 items
Load impedance:	50 Ω
Connector:	SMA (Jack)
Reference frequency output:	10 MHz, 1.5 Vp-p min., AC coupled, BNC
Reference frequency input:	10 MHz, 1.5 Vp-p min., AC coupled, BNC, automatically switched

External Clock

Frequency range:	150 MHz to 12 GHz 150 MHz to 12.5 GHz (Option 72)
Input level:	0.7 Vp-p to 1.5 Vp-p
Input waveform:	Sine wave
Main unit operating frequency range:	150 MHz to 12 GHz 150 MHz to 12.5 GHz (Option 72)

Patterns

Pattern Modes:	Can be selected from the 3 choices below. Pseudo random pattern (PRBS) Fully programmable pattern (WORD) Frame pattern (FRAME) (Option 70)
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PRBS

Pattern length:	$2^N - 1$, where N can be selected from among
7 choices:	N=7, 9, 10, 11, 15, 23 or 31

Number of stages N and generating function:

Number of stages	Generating function	Applied Standard
7	$X^7 + X^6 + 1$	ITU-T recommended V.29
9	$X^9 + X^5 + 1$	ITU-T recommended V.52
10	$X^{10} + X^7 + 1$	
11	$X^{11} + X^9 + 1$	ITU-T recommended 0.152
15	$X^{15} + X^{14} + 1$	ITU-T recommended 0.151
23	$X^{23} + X^{18} + 1$	ITU-T recommended 0.151
31	$X^{31} + X^{28} + 1$	

Mark ratio:	Can be selected from among 1/2, 1/4, 1/8, 0/8, 1/2B, 3/4, 7/8, or 8/8 The patterns 1/2B, 3/4, 7/8, and 8/8 are the logical inversions of the patterns 1/2, 1/4, 1/8 and 0/8 respectively.
AND bit Shift count:	1 bit
Word	
Pattern length:	1 to 8,388,608 (2^{23}) bits (with ALTERNATE OFF) 1 to 4,194,304 (2^{22}) bits (with ALTERNATE ON)
Logical inversion:	Possible
ALTERNATE mode:	Can be turned ON/OFF; When ON, can be switched to either of 2 patterns, A or B
Switching control:	Internal, external switching possible
Internal switching:	Done by front panel keys or GPIB
External switching:	Done by external alternate input signal

FRAME (Option 70)

Payload format:	3 types below can be selected Fully programmable (WORD) Pseudo random (PRBS) 0/1 continuous pattern + PRBS (CID)
Frame structure:	
When payload format is WORD or PRBS:	
Number of frames:	1 to 8,192 (with ALTERNATE OFF) 1 to 4,096 (with ALTERNATE ON) 1 frame steps
Number of lines in 1 frame:	1 to 16 (1 line steps)
Number of bytes in 1 line:	44 to 32,768
Number of overhead bytes in 1 line:	4 to (number of bytes in 1 line - 40 bytes), 4 byte steps
When payload format is CID:	
Number of bites in 1 line:	40 to 32,768, 4 byte steps
Number of overhead bytes in 1 line:	36 to (number of bytes in 1 line - integer quotient of 36) × 36, 36 byte steps
Number of 0/1 continuous pattern bits:	0 to (number of bytes in 1 line - number of overhead bytes in 1 line) × 8 bits, 1 bit steps
Stage Number of PRBS:	7, discontinuous parts may exist
Logical inversion:	Possible
ALTERNATE mode:	Can be turned ON/OFF (only when payload type is WORD or PRBS); When ON, can be switched to either of 2 patterns, A or B
Switching control:	Internal, external switching possible
Internal switching:	Done by front panel keys or GPIB
External switching:	Done by external alternate input signal
Error Addition	
Error addition mode:	Repeat, single, external
Repeat:	Error ratio 1×10^{-N} , N=4 to 9, bit error is added at a set interval
Single:	1 bit error is added with every error addition command
External:	1 bit error is added with every falling edge of an external error addition pulse input
Main Outputs	
Number of outputs:	Data, 2 patterns (DATA, $\overline{\text{DATA}}$) Clock, 3 patterns (CLOCK1, $\overline{\text{CLOCK1}}$, CLOCK2)
Data Outputs (DATA, $\overline{\text{DATA}}$)	
Number of outputs:	2 patterns (DATA, $\overline{\text{DATA}}$, complementary)
Format:	NRZ
Coupling:	DC
Amplitude range:	0.5 Vp-p to 2 Vp-p, 10 mV steps (TO 0 V, AC) 0.6 Vp-p to 1 Vp-p, 10 mV steps (TO -2 V)
(Option 15) :	0.5 Vp-p to 3 Vp-p, 10 mV steps (TO 0 V) 0.5 Vp-p to 2 Vp-p, 10 mV steps (TO AC) 0.6 Vp-p to 1 Vp-p, 10 mV steps (TO -2 V)
Offset range:	-2 V to +2 V, 10 mV steps (TO 0 V) -1 V to -0.6 V, 10 mV steps (TO -2 V)
(Option 15) :	-1 V to +1 V, 10 mV steps (TO 0 V) -1 V to -0.6 V, 10 mV steps (TO -2 V)
Rise/fall time:	30 ps max.
Load terminal conditions:	Can be selected as either DC coupled TO 0 V, TO -2 V or AC coupled
Offset setting level:	Can be selected as either HIGH, MIDDLE or LOW
Cross point variable:	ON/OFF selectable GPIB selectable
Load impedance:	50 Ω
Connector:	2.92 mm (plug)

Clock Outputs (CLOCK1, $\overline{\text{CLOCK1}}$)

Number of outputs:	2 patterns (CLOCK1, $\overline{\text{CLOCK1}}$, complementary)
Format:	RZ
Coupling:	DC
Amplitude range:	0.5 Vp-p to 2 Vp-p, 10 mV steps (TO 0 V, AC) 0.6 Vp-p to 1 Vp-p, 10 mV steps (TO -2 V)
Offset range:	-2 V to +2 V, 10 mV steps (TO 0 V) -1 V to -0.6 V, 10 mV steps (TO -2 V) (HIGH level reference)
Rise/fall time:	30 ps max
Load terminal conditions:	Can be selected as either DC coupled TO 0 V, TO -2 V or AC coupled
Offset setting level:	Can be selected as either HIGH, MIDDLE or LOW
Duty ratio variable:	ON/OFF selectable
Variable delay range:	± 400 ps, 1 ps steps (CLOCK2 output reference)
Load impedance:	50 Ω
Connector:	2.92 mm (plug)

Clock Output (CLOCK2)

Number of outputs:	1 pattern
Format:	RZ
Coupling:	AC (built-in DC blocking condenser)
Amplitude:	Approx. 1 Vp-p fixed
Offset:	0 V \pm 0.1 V fixed (MIDDLE level reference)
Waveform:	Rectangular wave
Rise/fall time:	30 ps max
Load impedance:	50 Ω
Connector:	2.92 mm (plug)

Trigger Signal Output

Output Signal:	Can be selected as either clock synchronization or pattern synchronization
Clock synchronization (1/32 CLK):	Clock frequency 1/32 divided output
Pattern synchronization (PATTERN):	Varies output position to any position in 16 bit units
Output level:	HIGH level 0 V \pm 0.2 V, LOW level -1 V \pm 0.2 V
Load impedance:	50 Ω to 0 V
Connector:	SMA

Auxiliary Output

1/2 Clock Output

Format:	RZ
Coupling:	DC
Output level:	HIGH level, 0 V \pm 0.2 V, LOW level -1 V \pm 0.2 V
Load impedance:	50 Ω to 0 V
Connector:	SMA

1/4 Rate Output

Output bit rate:	1/4 operating clock frequency
Number of pattern outputs:	4 patterns
Number of clock outputs:	1 pattern
Output skew:	± 150 ps max.
Output level:	HIGH level 0 V \pm 0.25 V, LOW level -1 V \pm 0.25 V
Load impedance:	50 Ω to 0 V
Connector:	SMA

Control Input

External Gate Input

Function:	Inhibits data output, inhibits at LOW level
Input level:	0 V/-1 V
Input pulse width:	At least 20 ns, or at least 64 x operating clock cycle, whichever is longer
Input impedance:	Approx. 50 Ω to 0 V
Connector:	BNC

External Alternate Input

Function:	In ALTERNATE mode, switches between patterns A and B; pattern A at HIGH level, Pattern B at LOW level
Input level:	0 V/-1 V
Input impedance:	Approx. 50 Ω to 0 V
Connector:	BNC

External Error Addition

Function:	When pattern error addition is external (EXT), 1 bit error is added for every fall edge of the input pulse
Input level:	0 V/-1 V
Input impedance:	Approx. 50 Ω to 0 V
Connector:	BNC

System Functions

Master/Slave Function

Function:	When used together with the D3286 Error Detector, allows the pattern settings of the D3186 and D3286 to be interlocked.
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Panel Lock:

possible

External Clock Generator Control Function

Function:	When external clock generator (SG) is used, the frequency and output level are controlled from the D3186
Connection method:	Dedicated GPIB connector

Remote Control

Interface:	GPIB (IEEE 488-1978)
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Calendar/Clock Function

Display:	Can be selected as either year/month/day/hour or day/hour/minute/second
File Function:	Built-in floppy disk drive
Functions:	Save, re-save, read in, erase and initialize
Saved data:	Operating conditions, pattern settings
Read in data:	Operating conditions, pattern settings
Disks used:	3.5 inch floppy disks, 720 KB (2DD), 1.2 MB (2HD), 1.4 MB (2HD)
Disk format:	MS-DOS [®] Rev. 4.0
File format:	Proprietary binary format

MS-DOS is a registered trademark of Microsoft Corporation.

General Specifications

Numerical value display:	Green 7 segment LED display
Set conditions memory:	After power has been ON for 12 hours, retained at least 2 weeks (backed up by secondary battery)
Operating temperature range:	0°C to +40°C +20°C to +30°C (Option 72)
Operating humidity range:	40% to 85% RH
Storage temperature range:	-20°C to +60°C
Storage humidity range:	30% to 85% RH (without condensation)
Power:	AC 100 V to 120 V, AC 220 V to 240 V (switches automatically) 48 to 63 Hz, sine wave
Power consumption:	550 VA max.
Mass:	42 kg max.
External dimensions:	Approx. 310 (H) \times 424 (W) \times 550 (D) mm

Standard Accessories

Name	Type	Stock No.	Quantity	Remarks
Power Cable	A01402	DCB-DD2428X01	1	
SMA-SMA Cable	DGM224-00700A	DCB-FF1211X01	7	
GPIO Cable	408JE-101	DCB-SS1076X02	1	
3 Pin- 2 Pin Converter Adapter For Power Plug	A09034	JCD-AL003EX03	1	
2.92 mm Adapter	02K121-K00S3	JCF-BJ001EX05	5	
User's Manual		JD3186 ED3186	1	Japanese English